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Applicant:	Toshiaki Sawada
U.S. National Stage Application of International Application No.	PCT/JP2004/013460
International Filing Date:	September 15, 2004
Attorney Docket No.	NAA236
Title:	Semiconductor Switch Circuit

March 16, 2006

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Commissioner of Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**INFORMATION DISCLOSURE STATEMENT**

Sir:


Pursuant to the duty of disclosure set forth in 37 CFR § 1.56, Applicant respectfully submits the following information disclosure statement.

The disclosed references are:

JP 03-029512; Japanese Patent Office; February 7, 1991, with English abstract.

Applicant respectfully requests that the Examiner initial the cited references shown on the enclosed form PTO-1449 and that the references be made of record in the present application.

Respectfully submitted,

  
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**Certificate of Mailing Under 37 CFR 1.10**

I certify that this Information Disclosure Statement and all enclosed materials are being deposited with the United States Postal Service on March 16, 2006 as "Express Mail," mailing label EV539508818US, in an envelope addressed to Mail Stop PCT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

  
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## INFORMATION DISCLOSURE STATEMENT

APPLICANT  
**Toshiaki Sawada**

FILING DATE

GROUP
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## U.S. PATENT DOCUMENTS

[illegible]

## FOREIGN PATENT DOCUMENTS

[illegible]

## NON-PATENT LITERATURE DOCUMENTS

*Exam. Initial	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	TRANSLATION	
			YES	NO

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP; draw line through citation if not in conformance and not considered. Include copy of this form with next communication with applicant.